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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/653,527	08/31/2000	Vladimir Berezin	08305/078001/99-23	4646

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EXAMINER	
WHIPKEY, JASON T	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/653,527	BEREZIN ET AL.	
	Examiner	Art Unit	
	Jason T. Whipkey	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-9,11-16 and 22-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,11-13 and 22-26* is/are allowed.

6)☒ Claim(s) *1-3,5,6,8,9,14-16,27 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-3, 5, 6, 8, 9, 14, and 15 have been considered but are moot in view of the new grounds of rejection.

Drawings

2. The amendment to the specification to obviate the objection to the drawings is approved. The objection to the drawings is withdrawn.

Specification

3. The amendment to the specification is approved and the corresponding objection is withdrawn.

Claim Objections

4. Claim 27 is objected to as failing to comply with 37 CFR 1.75(a) for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 27 recites the limitation "a gate of said first select transistor" on line 1. There is insufficient antecedent basis for this limitation in the claim. For examination purposes, the claim will be treated as if it reads, "a gate of said select transistor".

5. The amendment to claims 6 and 16 has overcome the objections to these claims. The objections are withdrawn.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 28 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Claim 28 specifies that the gate of the select transistor of the second pixel is connected to a third reset/select line. Parent claim 1, however, specifies that the gate of the select transistor is connected to a first reset/select line. The specification is silent with regard to both lines being connected to said transistor.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-3, 5, 6, 14, 15, and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen (U.S. Patent No. 5,869,857).

Regarding **claim 1**, Chen discloses an image sensor, comprising:

a plurality of pixels (see Figure 11A), each pixel having a photoreceptor (the shown photodiode; see column 7, lines 57-60) therein, a follower transistor (M1; see column 8, lines 2-4) connected to said photoreceptor, a select transistor (M2; see column 8, lines 11-12) connected to said follower transistor, and a reset transistor (M3) which controls applying a reset level (see column 8, lines 13-17);

a first bias line (V_{DD}) providing power to at least one of said transistors (M1) for a first pixel (shown in the upper left of the four pixels), and a second bias line (Vbias) providing power to another of said transistors (M3) different than said one of said transistors of said first pixel, such that said one and said another transistors are separately powered by separate bias lines, wherein a gate of said reset transistor of a first pixel is connected to a first reset/select line (Yn),

and a gate of said select transistor of a second pixel (shown in the lower left of the four pixels) is connected to said first reset/select line.

Regarding **claim 2**, Chen discloses:

said first bias line powers the follower transistor (V_{DD} is connected to M1) and said second bias line powers a reset transistor (Vbias is connected to M3).

Regarding **claim 3**, Chen discloses:

said photoreceptor is a photodiode (see column 7, lines 57-60).

Regarding **claim 5**, Chen discloses:

said sensor is an active pixel sensor (each pixel includes an amplifier M1 and is fabricated in CMOS; see column 7, line 63, through column 8, line 4), formed of transistors which are compatible with CMOS techniques.

Chen anticipates **claim 6**, but such a reading requires a different interpretation of claim 1, as follows:

a plurality of pixels (see Figure 11A), each pixel having a photoreceptor (the shown photodiode; see column 7, lines 57-60) therein, a follower transistor (M1; see column 8, lines 2-4) connected to said photoreceptor, a select transistor (M2; see column 8, lines 11-12) connected to said follower transistor, and a reset transistor (M3) which controls applying a reset level (see column 8, lines 13-17);

a first bias line (Yn) providing power to at least one of said transistors (M3) for a first pixel (shown in the upper left of the four pixels), and a second bias line (V_{DD}) providing power to another of said transistors (M1) different than said one of said transistors of said first pixel, such that said one and said another

transistors are separately powered by separate bias lines, wherein a gate of said reset transistor of a first pixel is connected to a first reset/select line (Yn[1]), and a gate of said select transistor of a second pixel (shown in the lower left of the four pixels) is connected to said first reset/select line;

wherein said sensor is an active pixel sensor (each pixel includes an amplifier M1 and is fabricated in CMOS; see column 7, line 63, through column 8, line 4), formed of transistors which are compatible with CMOS techniques.

wherein said select and reset transistors are connected to said first bias line (Yn) and said follower transistors are connected to said second bias line (V_{DD}; see Figure 11A).

Regarding **claim 14**, Chen discloses an active pixel sensor, comprising:

an array of pixels (see Figure 11A), each pixel comprising a photoreceptor (the shown photodiode; see column 7, lines 57-60), and at least first (M3) and second (M2) transistors associated with said photoreceptor in said each pixel, said first transistor connected to receive power from a first power supply source over a first line (Yn), and said second transistor connected to receive power from a second power supply line (Yn-1) totally separate from said first power supply line, wherein said first transistor of a first pixel and said second transistor of a

[1] The labeling of line Yn as both a first bias line and a first reset/select line is in accordance with the only correspondence that can be drawn between claim 6 and the specification of the instant application. Specifically, in Figure 2, the only common line that the select and reset transistors share is R/S Line N, which therefore must be the "first bias line providing power" recited in claim 6. VDD Line N-1 must therefore be the "second bias line" recited in claim 6. Therefore, in reading claim 1, the only line that can be the reset/select line (which is connected to the gates of both the reset transistor and the select transistor) is R/S Line N.

second pixel are connected to said first line (line Yn is connected to transistor M3 on the top row and M2 on the bottom row).

Regarding **claim 15**, Chen discloses:

said first transistor and said second transistor have drains which are not electrically connected (see Figure 11A).

Regarding **claim 27**, Chen discloses:

a gate of said select transistor is connected to a second reset/select line (Yn-1; see Figure 11A).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Merrill (U.S. Patent No. 5,614,744).

Claim 8 may be treated like claim 1. However, Chen is silent with regard to including a photogate, floating diffusion portion, and a transfer gate.

Merrill discloses a CMOS imager, wherein:

> said photoreceptor is a photogate (see column 1, line 50), and further comprising a floating diffusion portion (node FD; see column 1, line 51) in the substrate connected to said follower transistor, and further comprising a transfer gate (TX; see column 1, line 51), coupled between said photogate and said floating diffusion, which is activated to allow charge in said photogate to dump into said floating diffusion (see column 2, lines 11-13).

An advantage of using a photogate is that a high charge-to-voltage conversion gain is present, resulting in good low-light performance and minimal noise. For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Chen's image sensor include a photogate, as described by Merrill.

Regarding **claim 9**, Merrill further teaches:

> a reset diffusion (unlabeled and shown to the right of reset transistor R and connected to VDD) storing a reset level (VDD), and wherein said reset transistor is connected between said floating diffusion and said reset level.

13. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Okamoto (U.S. Patent No. 6,580,063).

Claim 16 may be treated like claim 14. However, Chen is silent with regard to including a steady-state current generator that switches between grounded columns and floating columns.

Okamoto discloses an image sensor, including:

> a steady state current generator (current source 809; see column 1, lines 37-38) for providing a first mode connecting columns to ground (column 1, lines 37-43) and a second mode which provides floating columns (activation of bias line 815 occurs at a specific time during the operation, as stated in column 2, lines 11-19; it is therefore inherent that a time exists when the line is inactive and the columns are floating).

An advantage of using such a current source is that the output signals from the pixels may be amplified as each column is read out. For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Chen's image sensor include a switchable steady-state current generator, such as the one described by Okamoto.

Allowable Subject Matter

14. Claims 7, 11-13, and 22-26 are allowed.

Regarding each of these claims, no prior art could be located that teaches or fairly suggests an active pixel sensor with each pixel containing a follower transistor, a select

transistor, and a reset transistor, wherein a second line is connected commonly to a plurality of followers in a first row and reset transistors in a second row.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

16. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Whipkey, whose telephone number is (571) 272-7321. The

examiner can normally be reached Monday through Friday from 9:00 A.M. to 5:30 P.M. eastern daylight time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber, can be reached at (571) 272-7308. The fax phone number for the organization where this application is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JTW

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May 31, 2005

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